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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,775	03/05/2002	Bruce E. Lavigne	100202224-1	8969

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EXAMINER	
WONG, WARNER	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/091,775	LAVIGNE ET AL.	
	Examiner	Art Unit	
	Warner Wong	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6-8,11,13-15,17-23 and 27-37* is/are pending in the application.

4a) Of the above claim(s) *2,3,5,9,10,12,16 and 24-26* is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 17-22* is/are allowed.

6)☐ Claim(s) *1,4,6-8,11,13,14,23 and 27-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 4, 6, 8, 11, 13, 23, 27-29 and 31-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuravleff (5,812,799) in view of Jeddeloh (US 6,295,592).

Regarding claim 1, Zuravleff describes a method of speculatively issuing memory requests in a network node while maintaining a specified packet order (fig. 1 data processing system), where the node (fig. 1, processor 30 and buffer management 10 combined) comprises:

receiving a first, then a second incoming packet for forwarding, wherein said first packet is received prior to said second packet (fig. 3a, "A1 request" and "A2 request" and fig. 5, #114, where I/O requests are queued in order of the request accordingly and that each request comprises the data packet, fig. 6, & col. 7, lines 19-20);

sending a first memory request corresponding to said first packet (fig. 3a, "A1 request");

sending a second memory request corresponding to said second packet prior to said network node receiving a first memory reply corresponding to said first memory request (fig. 3a & col. 9, lines 33-44, where "A2 request" (second memory request) is

sent prior to receiving "A1 reply" (first memory reply corresponding to said first memory request));

forwarding said first packet prior to forwarding said second packet (fig. 3a upon receiving "A1" reply" which indicates peripheral ready [fig., 11, #S40], the first packet is issued [fig. 11, #S60, fig. 6, #206 & col. 11, lines 3-5]; likewise for "A2 reply" for issuance of second packet);

Zuravleff describes:

receiving a second memory reply "A2 reply" from the memory (fig. 3a), but fails to explicitly describe the timeframe when the first packet is forwarded.

Jeddeloh describes the condition of 2 memory requests (col. 6, lines 20-21):

receiving a second memory reply prior to forwarding said first packet (fig. 8 & col. 6, lines 51-53, memory address module for the memory module receives the second address "Address 1" (reply), at clock cycle 106, before DATA 0 is transferred (forwarded) at clock cycle 110).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to explicitly describe the condition where two memory requests (with responses) were made before conducting a first packet transfer/forwarding as in Jeddeloh for the invention of Zuravleff.

The motivation for combining the teachings is that such explicit methodology provides an efficient pipelining of memory requests to memory devices (Jeddeloh, col. 2, lines 20-23).

Regarding claim 8, Zuravleff describes a network method comprising:

receiving a first and a second incoming packet for forwarding (fig. 3a, "A1 request" and "A2 request" and fig. 5, #114, where each request comprises the data packet, fig. 6, & col. 7, lines 19-20);

sending a first memory request corresponding to said first packet (fig. 3a, "A1 request");

sending a second memory request corresponding to said second packet prior to forwarding said first packet and prior to said second packet moving to a head of said transfer order queue (fig. 3a & col. 9, lines 33-44, where "A2 request" sent before memory receives A1 for processing receiving "A1" reply" which indicates peripheral ready [fig., 11, #S40], and prior to shifting second packet's request to head of (transfer order) queue, denoted by fig. 5, 114[0].. 114[n], for memory processing, denoted in fig. 3a where memory processes A2).

sending a second memory request corresponding to said second packet prior to receiving a first memory reply corresponding to said first memory request and prior to said second packet moving to a head of said transfer order queue (fig. 3a & col. 9, lines 33-44, where "A2 request" (second memory request) is sent prior to receiving "A1 reply" (first memory reply corresponding to said first memory request)).

Zuravleff describes:

receiving a second memory reply "A1 reply" from the memory (fig. 3a), but fails to explicitly describe the timeframe when the first packet is forwarded.

Jeddeloh describes the condition of 2 memory requests (col. 6, lines 20-21):

receiving a second memory reply prior to forwarding said first packet (fig. 8 & col. 6, lines 51-53, memory address module for the memory module receives the second address "Address 1", at clock cycle 106, before DATA 0 is transferred (forwarded) at clock cycle 110).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to explicitly describe the condition where two memory requests (with responses) were made before conducting a first packet transfer/forwarding as in Jeddeloh for the invention of Zuravleff.

The motivation for combining the teachings is that such explicit methodology provides an efficient pipelining of memory requests to memory devices (Jeddeloh, col. 2, lines 20-23).

Regarding claim 23, Zuravleff describes a network device comprising:

a means to receiving a first, then a second incoming packet for forwarding (fig. 3a, "A1 request" and "A2 request" and fig. 5, #114, where I/O requests are queued in order of the request accordingly and that each request comprises the data [packet], fig. 6, & col. 7, lines 19-20);

a means for sending a second memory request corresponding to said second packet prior to forwarding said first packet wherein said first packet is received prior to receiving said second packet (fig. 3a "A2 request" sent before receiving "A1" reply" which indicates peripheral ready [fig., 11, #S40] and inherently that the A1 request (packet) is received before the A2 request (packet) is received);

Zuravleff describes:

a means for receiving a memory reply "A0 or A1 reply" from the memory (fig. 3a), but fails to explicitly describe the timeframe when to send the first packet.

Jeddeloh describes the condition of 2 memory requests (col. 6, lines 20-21):

a means for receiving a memory reply prior to sending said first packet (fig. 8 & col. 6, lines 51-53, memory address module for the memory module receives an address "Address 0" or "Address 1", at clock cycle 100 & 106, before DATA 0 is transferred (forwarded) at clock cycle 110).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to explicitly describe the condition where two memory requests (with responses) were made before conducting a first packet transfer/forwarding as in Jeddeloh for the invention of Zuravleff.

The motivation for combining the teachings is that such explicit methodology provides an efficient pipelining of memory requests to memory devices (Jeddeloh, col. 2, lines 20-23).

Regarding claim 4, 11 and 27, Zuravleff further describes that the first memory request is to request I/O resources to forward said first packet (col. 3, lines 61-67).

Regarding claim 6, 13 and 28, Zuravleff further describes that the network node receiving a first memory reply prior to forwarding said first packet (fig. 11, step S40 & S60, where the buffer issues memory transaction request (fig. 6, which includes the data packet) only after the peripheral is ready via a reply command, fig. 3a).

Regarding claim 29, Zuravleff describes all limitations set forth in claim 28. Zuravleff further describes accepting a memory reply prompts the process to execute

and transfer the packet (assign network resource) (fig. 11, step S40 & S60, where the buffer issues memory transaction request (fig. 6, which includes the data packet) only after the peripheral is ready via a reply command, fig. 3a).

Regarding claims 31 and 33, Zuravleff further describes that the first packet and second packet are maintained in a transfer order queue (fig. 5, #114, where I/O requests are queued in order of the request accordingly and that each request comprises the data [packet], fig. 6, & col. 7, lines 19-20).

Regarding claims 32 and 34, Zuravleff further describes that the second memory request is sent prior to said second packet moving to a head of said transfer order queue (fig. 3a & col. 9, lines 33-44, where "A2 request" is sent prior to shifting second packet's request to head of (transfer order) queue, denoted by fig. 5, 114[0].. 114[n], for memory processing, denoted in fig. 3a where memory processes A2).

Regarding claim 35, Zuravleff further describes that the means for sending a memory request further comprises means for maintaining the transfer order of said first and said second packet (fig. 3a, where the buffer maintains the transfer order of the received requests corresponding to (first and second) packets for processing in the non-prioritized embodiment).

Regarding claim 36, Zuravleff further describes that the means for maintaining the transfer order of said first and said second packets comprises a transfer order queue (col. 6, lines 54-56, where the buffer (transfer order queue) maintains the transfer order of the received requests).

Regarding claim 37, Zuravleff further describes that said means for sending a memory request further comprise sending said memory request for second packet prior to said second packet reaching a head of said transfer queue ((fig. 3a & col. 9, lines 33-44, where "A2 request" (corresponding to packet not at a head of input queue) is sent prior to placing the A2 packet to said head of buffer (transfer queue), then forwarding to memory for processing).

2. **Claims 7, 14 and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuravleff in view of Jeddeloh as applied to claims 1, 8 and 23 above respectively, and further in view of Wakerly (5,875,466).

Zuravleff fails to describe:

Wakerly describes: the first packet comprises an internet protocol (IP) packet (col. 14, lines 56-66).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to describe received packets as IP packets.

The motivation for combining the teachings is that packets abiding to the well-known IP protocol standard are suitable to be used in existing Ethernet and FDDI networks (Wakerly, col. 14, lines 63-65).

Allowable Subject Matter

3. Claims 15 and 17-22 allowed.

Response to Amendment

4. Applicant's arguments filed 12/12/06 have been fully considered but they are not persuasive.

The applicant argues on p. 8, lines 11-19, (a) that the secondary reference of Jeddloh which describes a memory controller (fig. 1, #18) receiving memory requests to be contradictory to the primary reference of Zuravleff which describes a processor transmitting memory request, and (b) the Jeddeloh reference does not teach nor suggest that the same device is involved with both continuous request (see fig. 8, i.e, request 0 and request 1 from the same requesting device). The examiner respectfully disagrees.

The examiner understands that the Jeddeloh and Zuravleff references both teach pipeline processing for memory access and are combinable.

In rebutting (a), it is clear that in Zuravleff, the processor 'A' (with assistance by the non-block load buffer 10, see fig. 4) controls memory access (fig. 4, #50, DRAM memory devices), similarly in function to Jeddeloh's memory controller (fig. 1, #18), combined with the processor (fig. 1, #20), which also controls memory access (fig. 1, #12, memory module). It is also described that the Zuraveleff's processor 'A' receives the A1 and A2 memory requests (fig. 3a) before forwarding/transmitting such requests to the memory (col. 5, lines 58-67, processor receives instruction operations for memory requests), very much similar to Jeddeloh's memory controller receiving such memory requests before transmitting to the memory (fig. 3a of Zuraveleff can be compared with to fig. 8 of Jeddeloh).

In rebutting (b), the examiner concluded from the applicant's argument that the applicant misunderstood what the Examiner is trying to convey in the Office Action. Although Jeddeloh fails to explicitly describe that both request originate from the same device (i.e. the applicant argues that "request 0" may originate from video controller 31 and "request 1" may originate from the processor 20), Jeddeloh does suggests that the processor (one source) outputting both requests at a faster pace, therefore multiple requests are sent from the same source and the pipelining controller is needed to handle the requests (see Jeddeloh, col. 1, lines 37-55). The above Office Action has been updated slightly for clarification.

Hence independent claims 1, 8 and 23 stand rejected.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Warner Wong whose telephone number is 571-272-8197. The examiner can normally be reached on 6:30AM - 3:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Warner Wong
Examiner
Art Unit 2616

WW

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SUPERVISORY PATENT EXAMINER